08:30	**FPGAworld 2019** **Registration Sep 19th, DTU (SCION), Building 372, Diplomvej 2800 Lyngby**
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09:00	**Conference opening** Professor Lars Dittmann, Technical University of Denmark and Lennart Lindh, FPGAworld
09:15-10:00	 **Keynote** **Did Europe miss the start in AI Technology?** **Keynote speaker:** Jens Stapelfeldt, Xilinx, CA **Abstract:** What does the Scandinavian AI landscape look like in comparison to other European and international countries, in which areas is progress already being made, and what can be done tomorrow? Artificial Intelligence (AI) has been the megatrend in the technology world for several years now. This talk gives a short overview of the AI/ML (machine learning) landscape and where Scandinavia stands in comparison. One trend in AI technology is the integration of AI in "Edge" Devices, i.e. in the device on site! One focus of the talk is to show what is possible today with optimized CNN networks and what we can expect in the next generation. We will also discuss "how do we get 20TFOLP into an SSD network under 10W to run without going into the cloud and consuming hundreds of Watts"? Session Chair: Professor Lars Dittmann, Technical University of Denmark
10:00-10:30	**Coffee Break & Exhibition**
10:30-12:00	Industrial/Product Presentations Session Chair: Lennart FPGAworld **A: VHDL-2019 - What is important and Why** Jim Lewis, SynthWorks Design Inc and chair of the IEEE VHDL Working Group, USA (more info) **C: Identifying & Correcting difficult to find RTL problems earlier** Adam Taylor, Blue Pearl Software **C: Functional Safety for FPGAs** Stefan Bauer, Mentor Booked
12:00-13:00	**Lunch Break & Exhibition**
13:00-13:30	**FPGA events during the year that has gone and gossips** **Mike Dini talk,** Dini Group, USA Session Chair: Rolf Sylvester-Hvid, Aktuel Elektronik, Denmark

13:30-14:30	Industrial/Product Presentations Session Chair: Lennart FPGAworld **C: Everything you need to accelerate innovation** Yehoshua Shoshan, Innofour **A: How to accelerate the development of your embedded visions system?** Andrea Leopardi, BitSim, Sweden (more info)
14:30-15:00	**Coffee Break & Exhibition** SILEXICA
15:00-15:45	**Keynote** **FPGA, the mainstream accelerator of choice for the FinTech Industry** **Keynote speaker:** David Clarke, Intel PSG **Abstract:** The increase in the requirement for greater levels of compute density driven by increasing regulatory pressure is critically driving the need for acceleration in the financial data-centers. For a many year's, CPU's have been the preferred processing engine because of their programmability and their faster implementation of algorithms. With the increased need for deterministic latency, near real-time option price and trends calculations the ultra-flexible FPGA is becoming the most efficient acceleration processing platform in Fintech. Alternative technologies such as GPU, struggle to deliver the performance, power and usability required to scale as an accelerator across data-center. The presentation focus on how the barriers is removed paving the way for adoption of FPGA in FSI (Financial Service Industry) by developing high level abstraction financial libraries and frameworks to allow fast time-to-market development of OpenCL/HLS algorithms. The FPGA is becoming the mainstream accelerator in the FSI data-centers. Session Chair: Lennart FPGAworld, Technical University of Denmark
15:45 -	**Go Home Drink in Exhibibition Hal** DTU

Exhibitors and Product Presenters Copenhagen and Stockholm	DTU, Technical University of Denmark ÅF, Sweden Aktuel Elektronik, Denmark Elektroniktidningen, Sweden Dini Group, USA Intel PSG, USA Mentor – A Siemens Business XILINX, USA SILEXICA, Germany GOWIN, China	PyramidTech, USA Lattice, USA Avnet Silica, Denmark Avnet Silica, Sweden Synopsys, USA BitSim, Sweden Blue Pearl Software, USA Xiphera, Finland SynthWorks, USA VSYNC Circuits, Israel	Bitvis and CGI, Norway Arrow, Europe Silicon Labs, Finland InnoFour, Netherlands Synective Labs, Sweden Blue Pearl Software Inc, USA MathWorks, USA Motion Control, Sweden AGSTU FPGA Education (Yrkeshögskola), Sweden

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Stockholm 15 September and Copenhagen 17 September

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VHDL-2019 - What is important and Why

Abstract: VHDL-2019 adds numerous features that are targeted at verification improvement. These include: interfaces, protected type improvements, an API for Assert and PSL, and conditional compilation. Interfaces allow models to handle an interface connectivity abstractly. Protected types are used to create verification data structures, such as scoreboard, coverage modeling, ... The improvements provide the next step in modeling capability. The API for Assert and PSL allows tests to get a count of errors from these sources. Jim is chair of the IEEE VHDL Working Group.

Event: Stockholm, Copenhagen

From: Jim Lewis, SynthWorks Design Inc, USA

Identifying & Correcting difficult to find RTL problems earlier

Abstract: All engineers know the earlier we identify an issue in our design, the easier and less costly it is to correct. The worst issues are intermittent and manifest late in test or worse in the field. These late issues lead to long hours and stress in the engineering team. This session will explore common design issues which can cause these hard to find late issues, how we can address them along with outlining how they can be identified easier using Blue Pearl's Visual Verification Suite

Presenter: Adam Taylor, Blue Pearl Software, USA

Company website: https://www.bluepearlsoftware.com/

Functional Safety for FPGAs

Abstract: Everybody is talking about and many companies are jumping on the functional safety train. The latest industry study from the Wilson Research Group shows, that almost 2/3 of today's European FPGA design projects are used within a safety application, i.e. autonomous driving or airplanes. Such safety applications require a high quality and a high reliability of the FPGAs. But the truth is, that more than 70% of these FPGA designs still have non-trivial bugs which escape to production. Functional Safety is driving down risk of Electrical and Electronics malfunctioning due to failures. Standards like ISO 26262 or IES 61508 focus on two areas of faults: Systematic Faults and Random Faults. In this presentation Stefan Bauer, one of Mentor's verification experts, will give an introduction to the ISO 26262 standard and how Mentor's overall functional safety flow can help to verify Systematic Faults and Random HW Faults.

Event: Stockholm, Copenhagen
Presenter: Stefan Bauer

Comapany website: https://www.mentor.com/

Everything you need to accelerate innovation

Abstract: Embedded software is in virtually all the products we come in contact with every day. As a result, the use of embedded software is quickly infringing on hardware's dominance in the product development process. This presentation will cover the challenges in today's embedded software development and how we can help organizations with a unified solution that divers project transparency through real-time aggregated management information.

Event: Stockholm, Copenhagen

From: Yehoshua Shoshan, InnoFour

Comapany website: www.innofour.com

How to accelerate the development of your embedded visions system?

Abstract: It's a huge task to cover everything from collecting data from for example RGB- or IR-sensors, process and analys the data and then, perhaps to make decisions depending on the result. BitSim has developed a platform integrating both sequential (CPU) and parallel (FPGA) processing to make the implementation of all these steps easier and faster. With this platform it is possible to integrate into a single application different types of algorithms, from embedded vision to Deep Learning. It can for example be used in Smart Farming, to monitor the

Event: Stockholm, Copenhagen

From: Andrea Leopardi, BitSim AB, Sweden

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